EE/CPRE/SE 491 - sddec24-13

ReRAM Compute ASIC Fabrication

Weekly Report 2

2/7/23/24 - 2/13/24

Client: Prof. Henry Duwe

Advisor: Prof. Cheng Wang

Team Members:

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog digital designer
- Nathan Cook – Main client liaison, mixed analog digital designer
- Jason Xie – assistant documentation editor, main digital designer

Weekly summary:

This week, we were able to get all tools running on our personal machines, allowing us to begin checking out the programs. During our client and advisor meeting, we further identified more micro level deliverables and gained a clearer vision of our project. We also gained access to the research lab that has the physical machines in Durham 310 and were able to start using those as well.

Past Week Accomplishments

- Installed and ran all required open-source software, using a combination of WSL and windows
- Installed and ran all required open-source software on Ubuntu
- Looked into ADC (Analog to Digital Converter) design methods to talk to our client and advisor about which method or what specific performance goals they would like out of the device
- Accessed Durham 310 and began working on their physical machines

Individual Contributions:

Team Member	Contributions	Weekly hours	Total Hours
Konnor Kivimagi	Researched more about ReRAM. Got the tool flow up and running from a virtual computer	8	14
Gage Moorman	Succeeded in getting open-source tools running, created test inverter Verilog code and test bench	8	14
Nathan Cook	Got all the software installed and running, did some research on ADC types and design uses	8	14
Jason Xie	Finished setting up tools and began creating an inverter	6	12

Pending Issues:

- Researching and deciding what route to take when designing the DAC and ADC.
    - We have ideas for the ADC design, a SAR design specifically. Duwe mentioned for DAC design to use Bit Serial computation (will further research on BSC)
- Creating an inverter to run through the tool flow to provide proof of concept.
    - Wanted to get to this last week but had issues with software installing and permissions

Plans for the coming week:

- Gage Moorman
    - Practice using the tools and workflow
    - Run a practice tool flow using inverter
    - Research ADC and DAC architectures that would be best fit for our design
- Konnor Kivimagi
    - Dive into the tools to gain a better understanding of their inner workings
    - Spend some time researching different methods to create different analog devices
    - Create some simple working test circuits and bring them through the tool flow
- Nathan Cook
    - Begin using tools and designing a simple hello world type of circuit
    - Look into DAC and ADC function to get a better understanding of the technology and how it would be implemented.
- Jason Xie
    - Run a practice tool flow using inverter
    - Begin researching common circuits that could satisfy project requirements

Summary of Advisor Meeting:

During our meeting this week, we got more specifics on the overall deliverables that would be expected and the smaller micro level ones. Among the overall deliverables the client and advisor would like to have a design to be GS2 precheck approved, and simulations

showing the devices working correctly making it plausible to be manufactured and realized physically.